Art Unit: 2812

Serial No.: 09/944,522 - 5 -

## **REMARKS**

Claims 1-13 were previously pending in this application. By this amendment, Applicant is canceling claim 3 without prejudice or disclaimer. Claims 1, 6, and 11 have been amended. New claims 17-18 have been added. As a result claims 1, 2, 4-13, 17 and 18 are pending for examination with claim 1 being an independent claim. No new matter has been added.

## Rejections Under 35 USC §102

Claims 1-2, 4, 6-7 were rejected under 35 U.S.C. §102(b) as being anticipated by Iwamuro, U.S. Patent No. 5,936,267 (hereinafter "Iwamuro"). In response, Applicant has amended the claims and submits the following remarks with respect to the cited reference.

Iwamuro is directed to an insulated gate thyristor that are emitter switched (Col. 3, lines 16-21 and Col. 5, lines 35-47). These devices are MOS-gated devices that are created using a silicon (Si) substrate material (Col. 6, lines 27-31 and Col. 6, line 49 through Col. 7, line 18).

Independent claim 1 cites a method of forming at least one doped layer of a thyristor comprising providing a semiconductor crystal of a single crystalline carbide material, the semiconductor crystal having a crystal structure and forming a gate turn-off thyristor device having a plurality of layers including a layer that forms an upper base of the thyristor device, and introducing impurities in the crystal structure to form the upper base layer after the crystal structure has been formed.

Iwamuro does not anticipate independent claim 1. In particular, Iwamuro does not disclose an act of "providing a semiconductor crystal of a single crystalline carbide material," as recited in claim 1. In particular, Iwamuro uses a silicone substrate, not a semiconductor crystal of a single crystalline carbide material as recited. Further Iwamuro does not disclose an act of "providing a semiconductor crystal..., the semiconductor crystal having a crystal structure and forming a gate turn-off thyristor device," as recited in claim 1. Iwamuro is primarily concerned with silicon MOS-gated thyristors, not gate-turn-off thyristors (GTOs). Therefore, Iwamuro does not anticipate claim 1 and the rejection should be withdrawn. Claims 2, 4-13 and 17-18 depend from claim 1 and are allowable for at least the same reasons.

Claim 17-18 were added to further define Applicant's contribution to the art. These claims are allowable for at least the same reasons as discussed above with reference to claim 1.

Serial No.: 09/944,522

-6-

Art Unit: 2812

## Rejections Under 35 U.S.C. §103

Claims 3 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Iwamuro in view of Edmond, et al. U.S. Patent No. 5,087,576 (hereinafter "Edmond"). As discussed above with respect to the Iwamuro reference, claims 3 and 5 are patentable for at least the same reasons as claim 1. Further, Edmond does not teach or suggest the missing limitation as discussed above with respect to Iwamuro. For at least these reasons, the rejection should be withdrawn.

## **CONCLUSION**

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50/2762.

Respectfully submitted, Tatsing P. Chow, et al., Applicants

Rv./

Edward J. Russavage, Reg. No. 43,069 LOWRIE, LANDO & ANASTASI, LLP

One Main Street

Cambridge, Massachusetts 02142

United States of America Telephone: 617-395-7000 Facsimile: 617-395-7070

Docket No. R00434/70008 Date: September 15, 2003